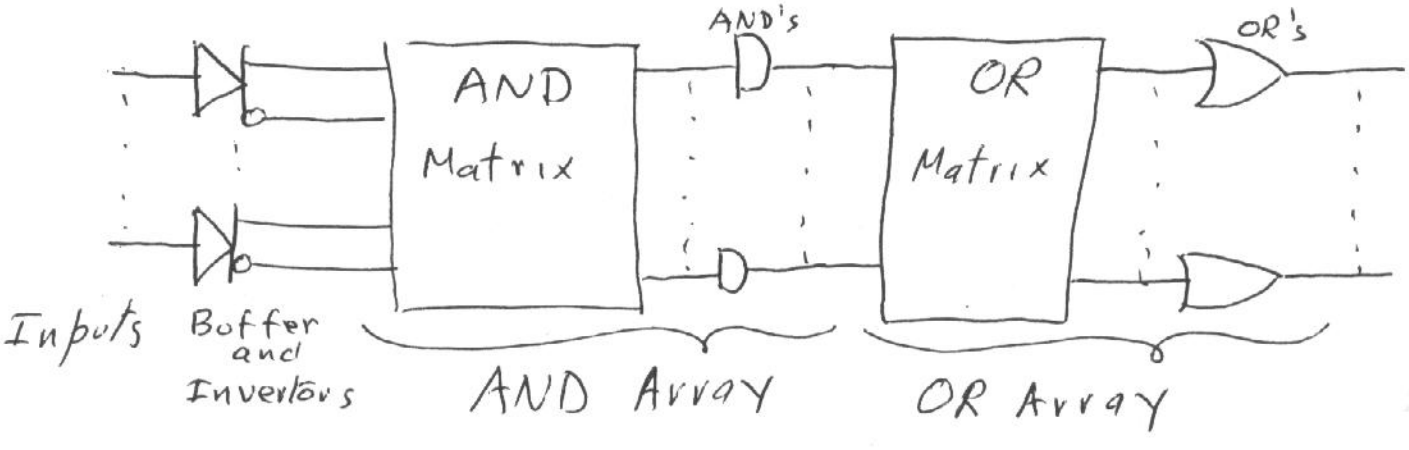
Programmable Logic Devices (PLD's)

= an IC that can be programmed ("burned") during or after manufacture to perform a variety of functions. if manufacturer programs ⇒ "mask" programmed
" end user " ⇒ "field" programmed.

Subject is an alphabet soup of acronyms with many companies making many devices. A first try at characterizing might be

1. Low density (up to say 28 pins), general purpose devices, PLA's and PAL's (generically both are PLD's). Add a prefix "E" in front to get "evasable" devices. Add another E (to get EE or E^2) to get "electrically evasable" devices.
2. Medium-high density (40 pins and up) general purpose devices such as CPLD's and FPGA's.
3. Function specific devices designed and programmed for a specific task – hence denoted as ASIC's.

Generic architecture for combinational PLD's is



Distinctions re architecture:

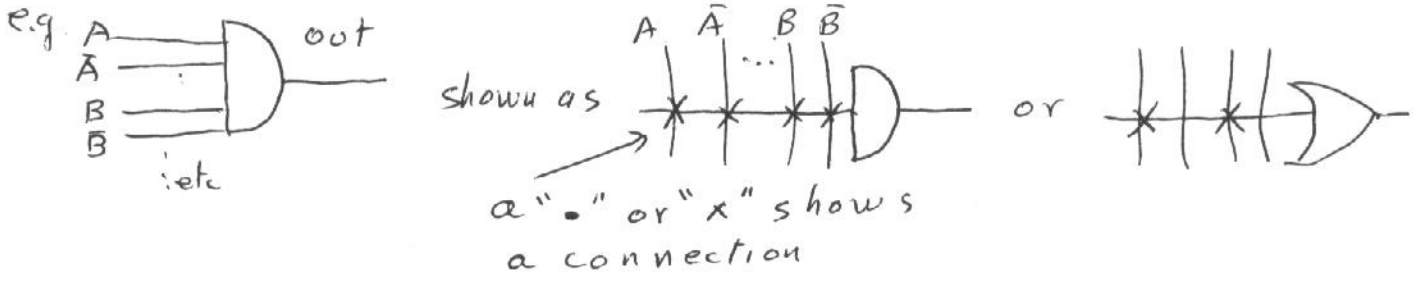
Device Type	AND Array	OR Array
PROM	fixed	programmable
PAL	programmable	fixed
PLA	programmable	programmable

(Note: PAL is a registered trademark owned by AMD)

Programing may be "one time only" accomplished by "blowing" metallic connections in the devices. Alternately, the connections in some devices are created by electrically causing "channels" to appear. These channels can be erased (prefix "E") by shining UV light on them or electrically (prefix "EE").

Drawing convention

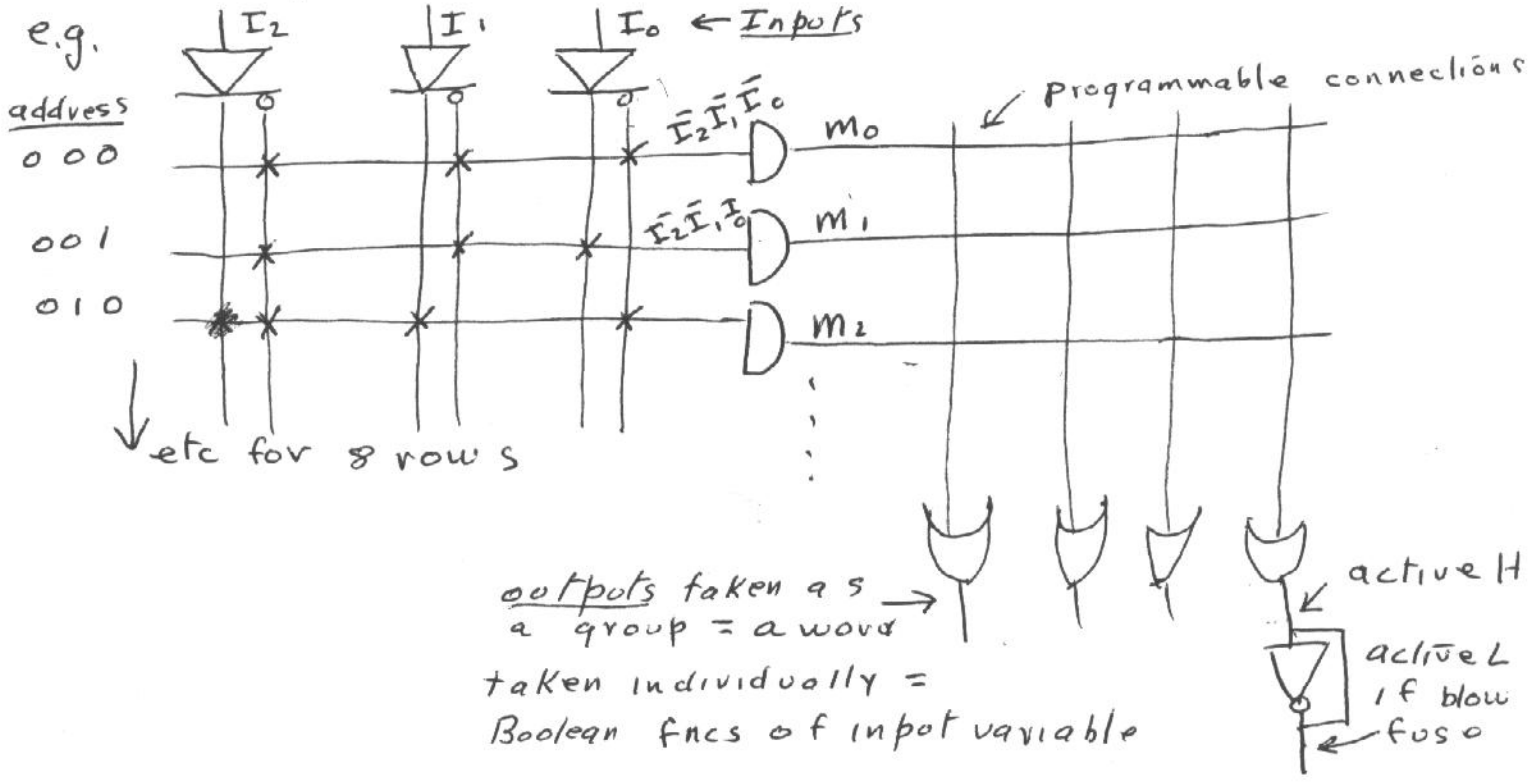
Since there may be many gates with many inputs, a somewhat different way of showing connections is used:



PROM: first programmable IC. May be mask programmed by manufacturer and sold as a ROM (read only memory). May be end user programmable and sold as a PROM. May be erasable by end user and reprogrammed - sold as a EPROM (UV erasable) or as a EEPROM (electrically erasable)

PROM's have a fixed AND array which generates all min-terms of the input variables and a programmable OR array which sums the needed min-terms.

e.g.



Typical devices

	# Input lines	# Output lines	Referred to as.
27519	5 (32 addresses)	8	32/8 bit bytes
2716	11 (2048 ")	8	2K bytes
2764	13 (8192 ")	8	8K bytes
27128	14 (16K ")	8	16 K bytes
27256	15 (32K ")	8	32 K bytes
27512	16 (64K ")	8	64K bytes
NM27C240	18 (256K ")	16	256K 16 bit words

etc, many types from many vendors

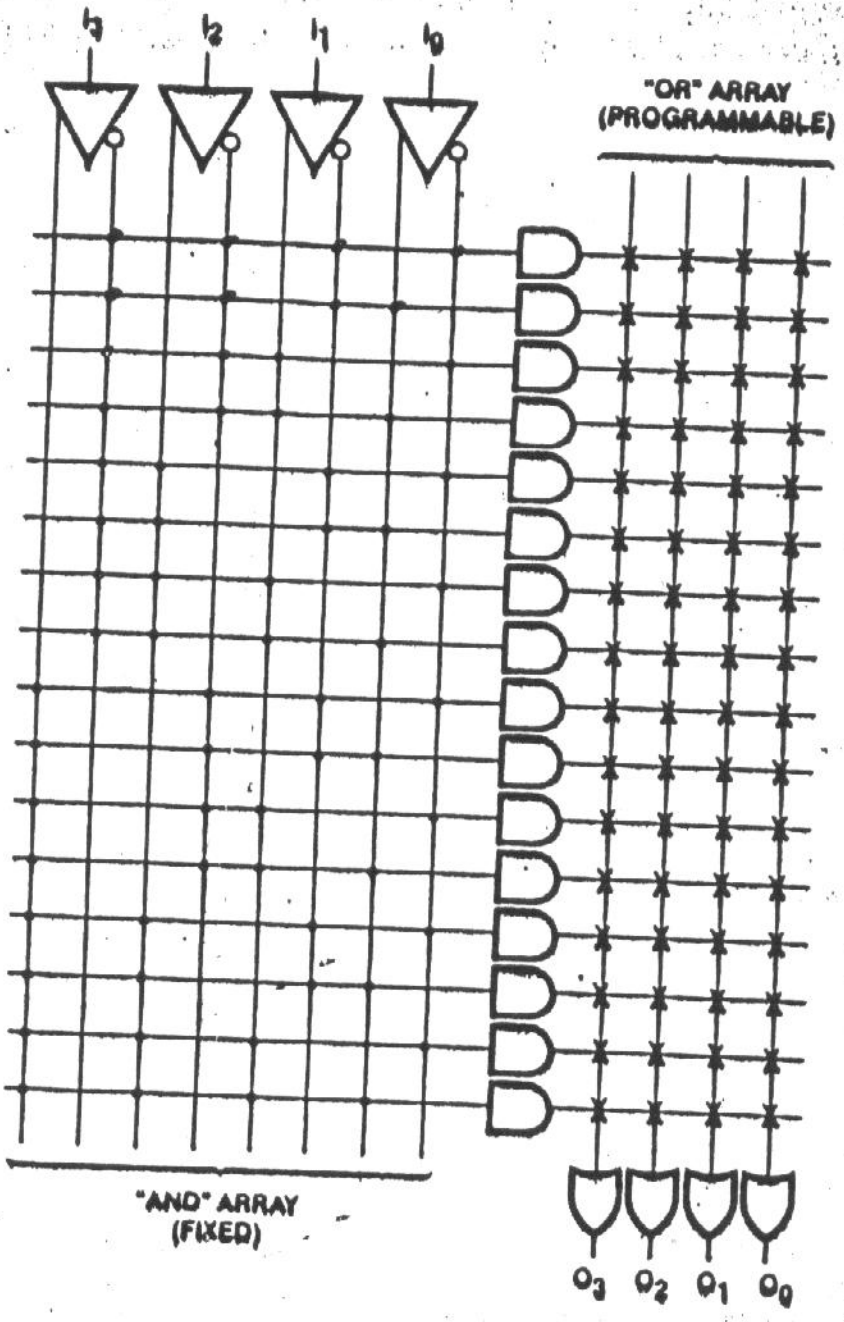
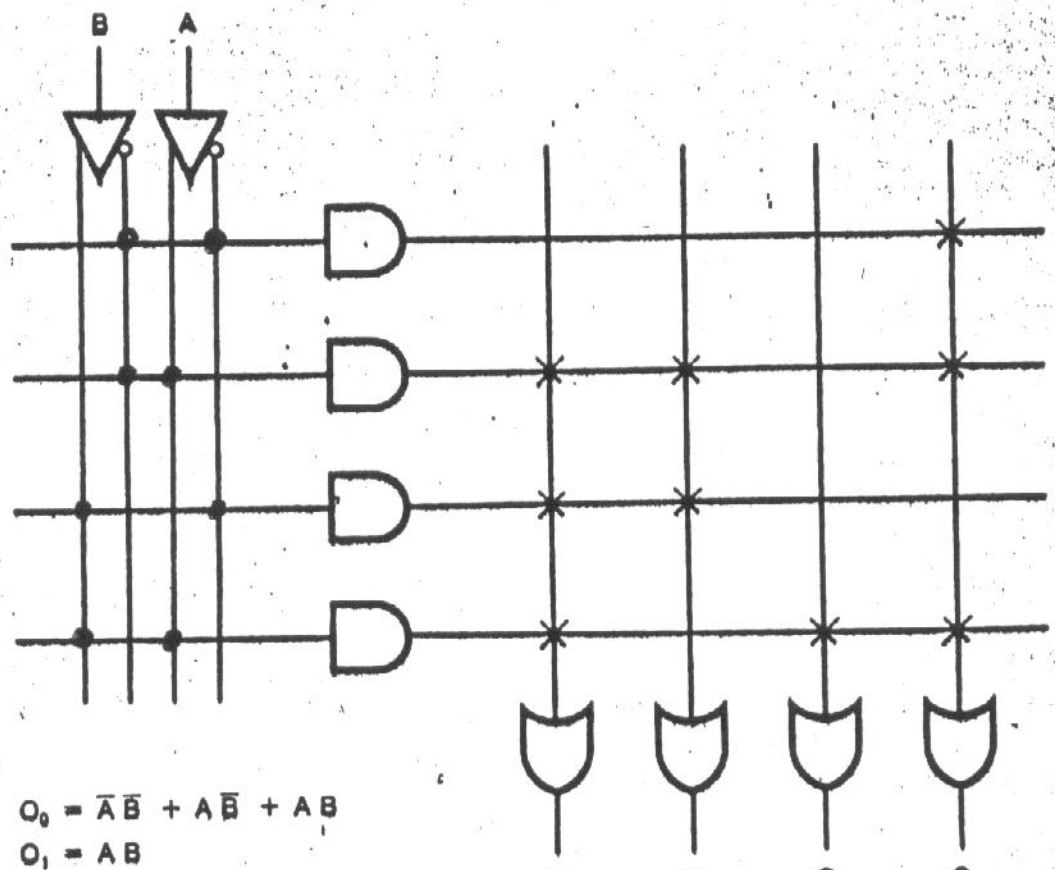


Figure 3-7. PROM conceptual logic diagram: a fixed AND-array followed by a programmable OR-array.



$O_0 = \overline{A}\,\overline{B} + A\,\overline{B} + A\,B$

$O_1 = A\,B$

$O_2 = A\,\overline{B} + \overline{A}\,B$ (Exclusive – OR)

$O_3 = A\,\overline{B} + \overline{A}\,B + A\,B$

Figure 3-8. Diagram of a programmed PROM showing output logic equations.

TABLE 5.4 BINARY-TO-GRAY CODE TRUTH TABLE

Decimal Number	Binary $B_3B_2B_1B_0$	Gray Code $G_3G_2G_1G_0$
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

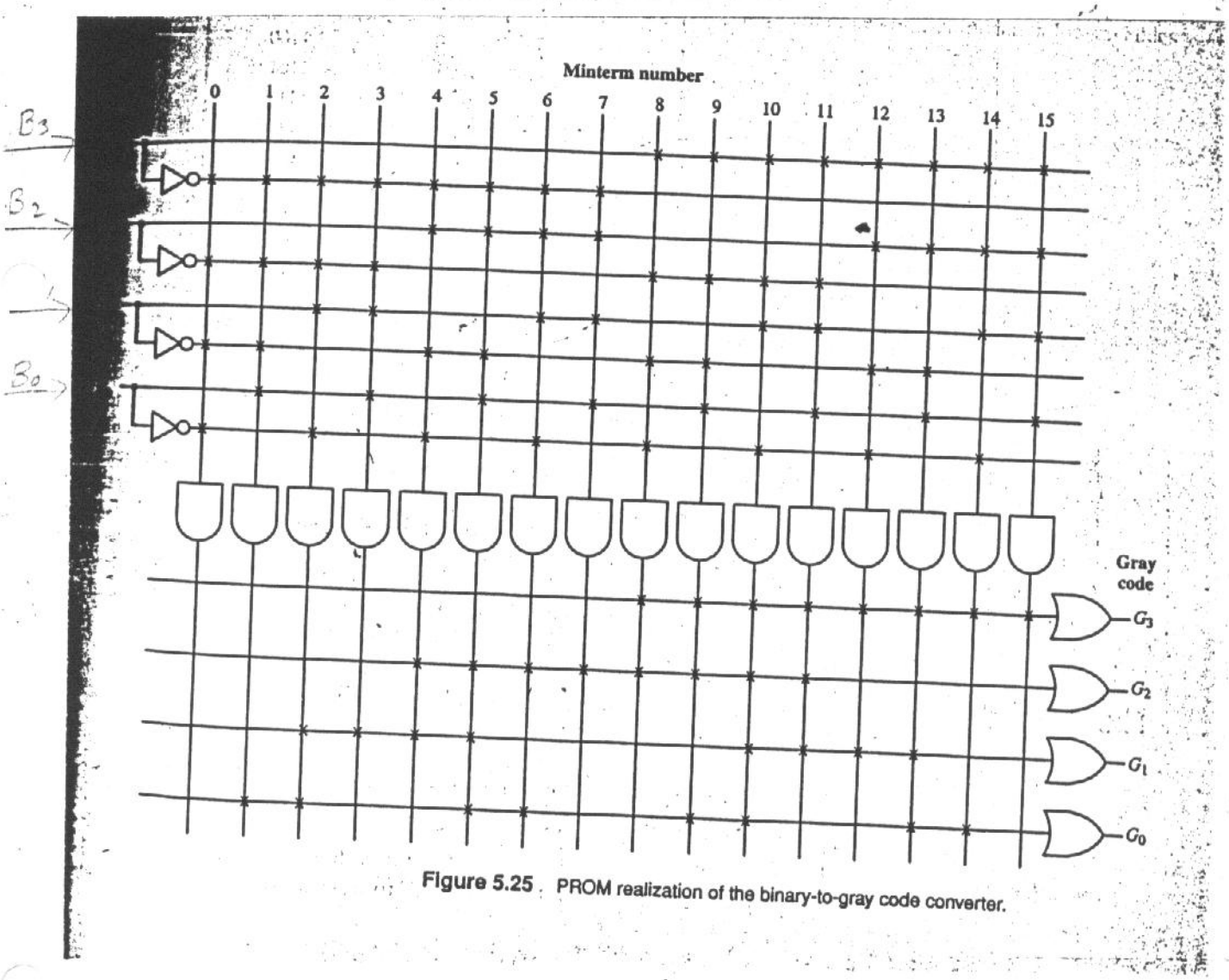


Figure 5.25 PROM realization of the binary-to-gray code converter.

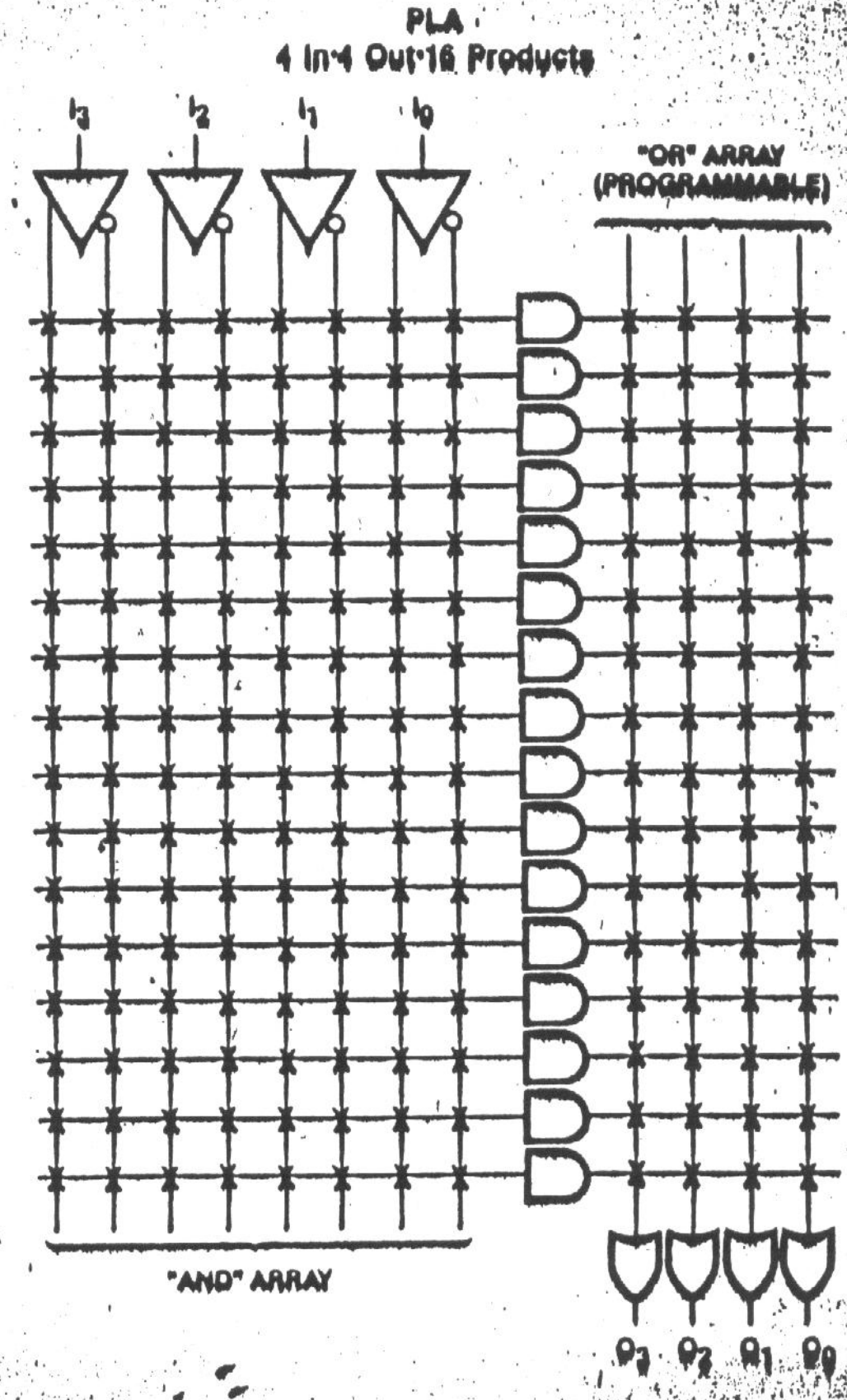


Figure 3-9. FPLA conceptual logic diagram: a programmable AND-array followed by programmable OR-array.

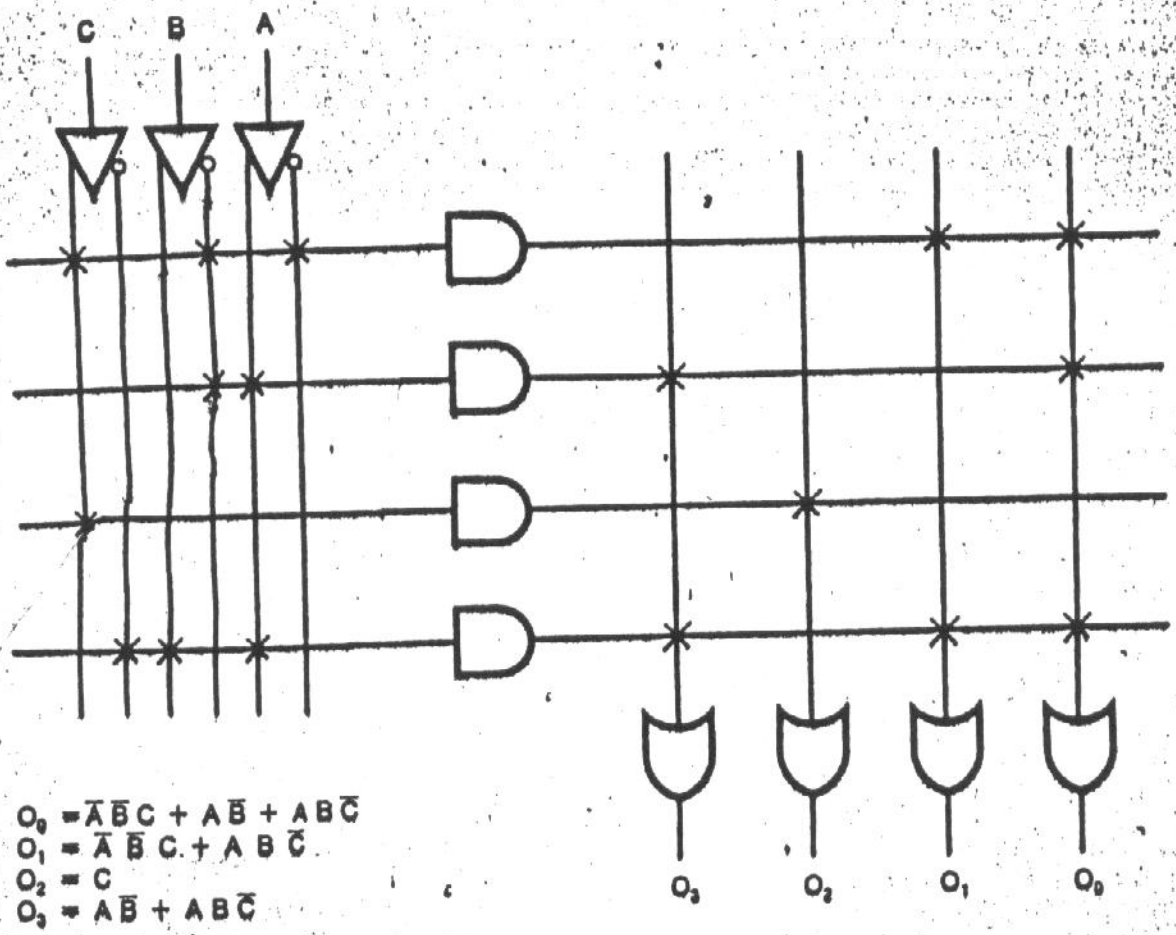
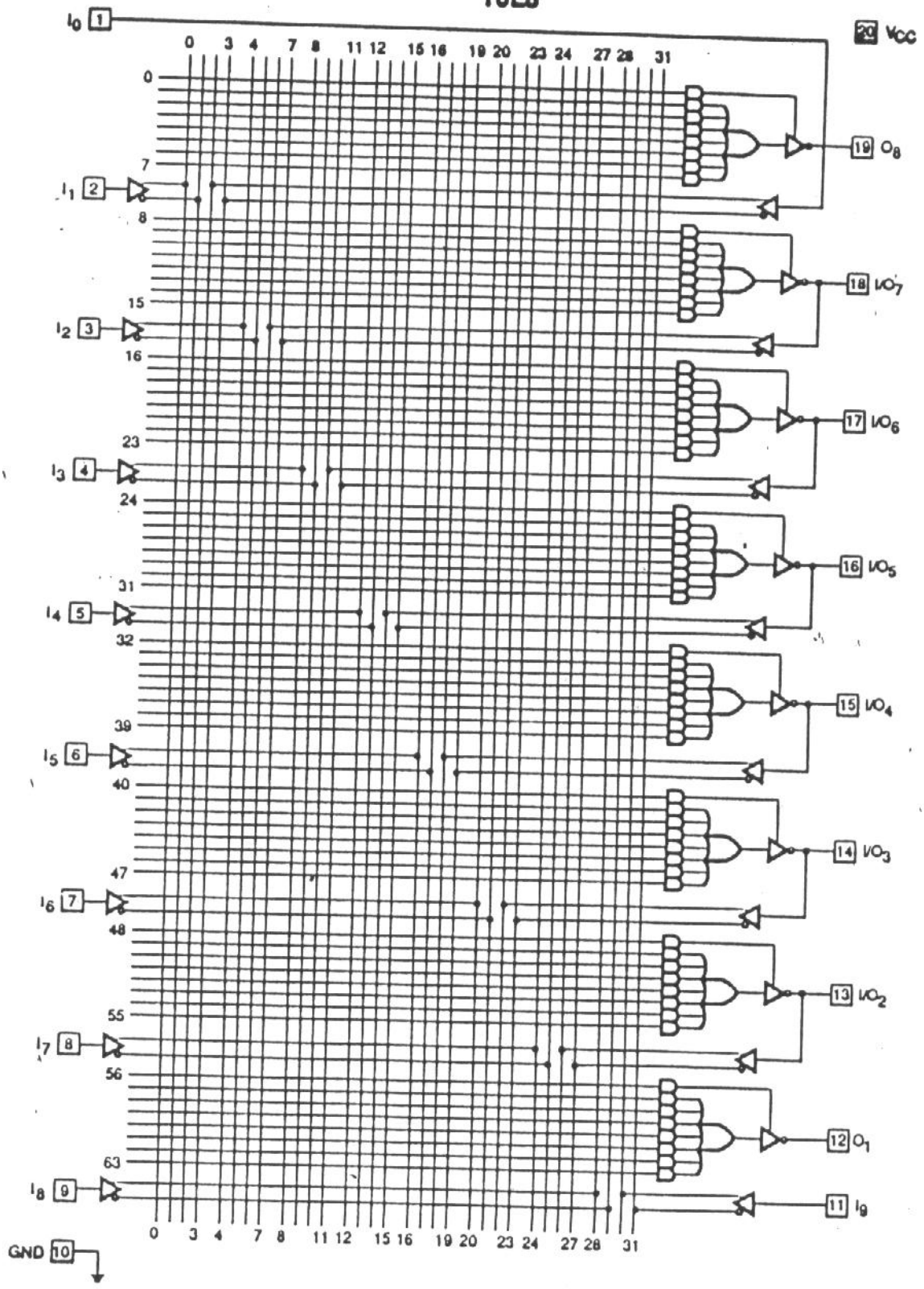


Figure 3-10. Diagram of a programmed FPLA showing output logic equations.

16L8



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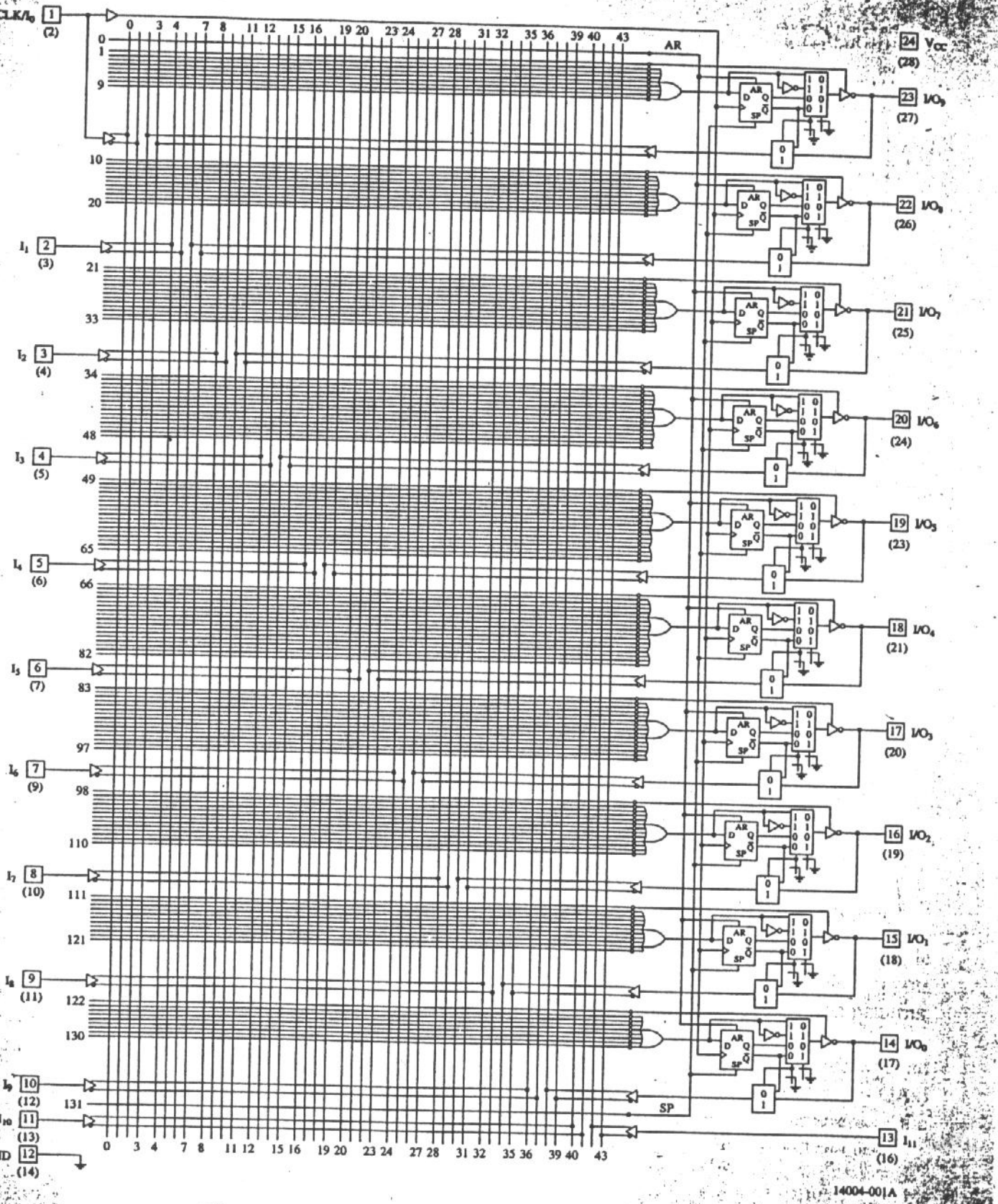

Figure 11.14 Complete PAL22V10 PLD logic diagram [2]. Copyright © Advanced Micro Devices, Inc., 1993. Reprinted with permission of copyright owner.