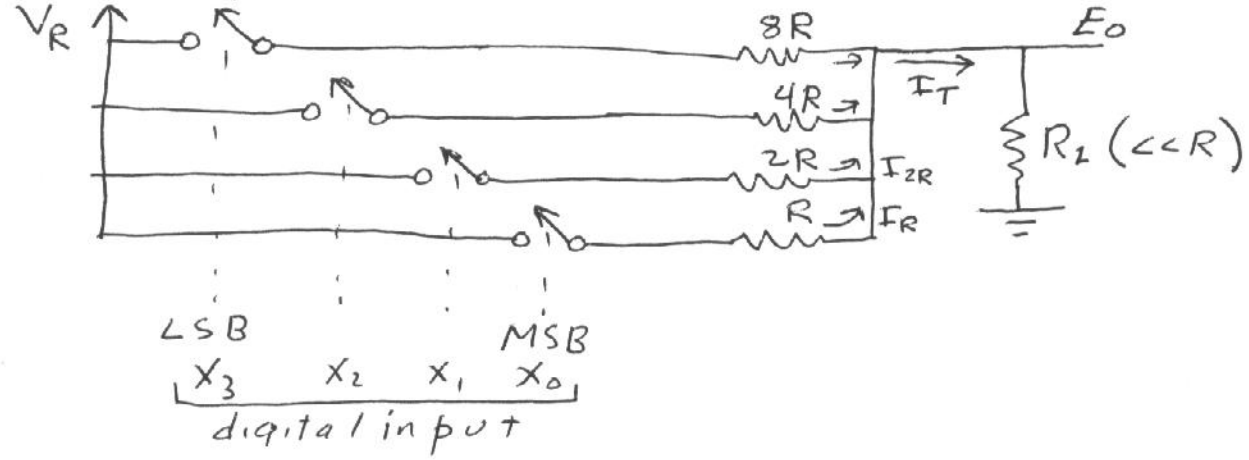
D/A Conversion

D/A ⇒ circuit accepts a digital word in and outputs a corresponding analog voltage or current.

Basic elements in most D/A's

1. precision voltage reference
2. set of precision resistors
3. set of analog switches which are digitally controlled
4. means for summing current contributions

Simplest type of D/A



Choosing R_L small means E_o will be much less than V_r. Hence current contributions to I_T can be approximated (when associated switch is closed) as

$$I_R = \frac{V_R - E_o}{R} \doteq \frac{V_R}{R} \quad \text{etc}$$

so $$I_T = I_R + I_{2R} + \cdots = V_R\left[\frac{X_3}{8R} + \frac{X_2}{4R} + \frac{X_1}{2R} + \frac{X_0}{R}\right]$$

$X_i = 1$ switch closed

$X_i = 0$ switch open

or $$I_T = \frac{V_R}{R}\left[\frac{X_3}{8} + \frac{X_2}{4} + \frac{X_1}{2} + \frac{X_0}{1}\right]$$

and so $E_o = I_T \cdot R_L$ or

$$E_o = \underbrace{\left(\frac{R_L}{R} V_R\right)}_{\text{overall scale factor}} \underbrace{\left[\frac{X_3}{8} + \frac{X_2}{4} + \frac{X_1}{2} + \frac{X_0}{1}\right]}_{\text{binary weighted current contributions}}$$

obviously can be expanded for more bits

e.g. if have $X_3 \cdots X_0 = 0110$ with $R_L = .1R$ and $V_R = 8\ V$

get $E_o = (.1 \cdot 8)\left[\frac{0}{8} + \frac{1}{4} + \frac{1}{2} + \frac{0}{1}\right] = (.8)\left(\frac{3}{4}\right) = 0.6\ V$

max E_o (i.e. F.S.) $= (.8)\left(\frac{15}{8}\right) = 1.5\ V$ full scale

smallest non-zero output would be:

$E_{o_{min}} = (.8)\left(\frac{1}{8}\right) = .1\ V$ = resolution, i.e. change in output corresponding to change in LSB of input.

From this see that

# bits	# states	equivalent resolution	
4	16	6¼ %	(6%)
8	256	0.39 %	(.4%)
10	1024	0.097%	(.1%)
12	4096	0.025%	(.025%)

From practical view point above scheme has draw backs:

1. No output buffering, i.e. any external load on R_L could affect scale factor
2. Requirement that R_L be low for good current summing and high for reasonable output levels are incompatible.
3. Range of resistor values becomes large for more bits.
4. Need latch to hold on to input word.

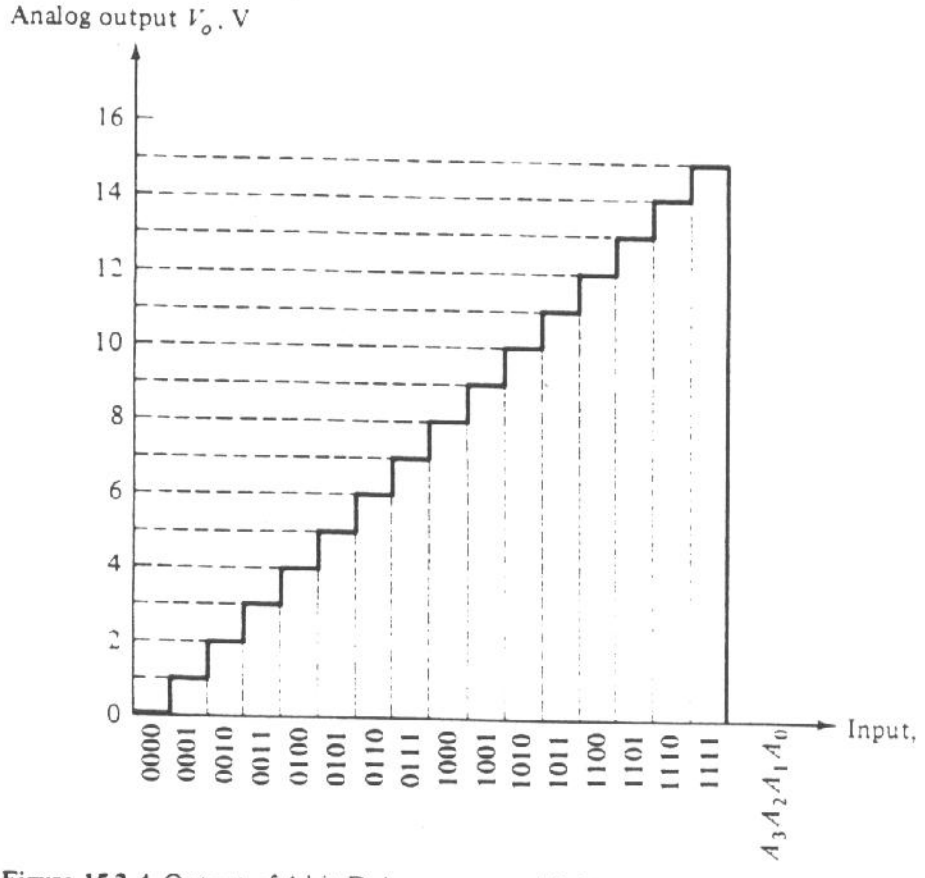
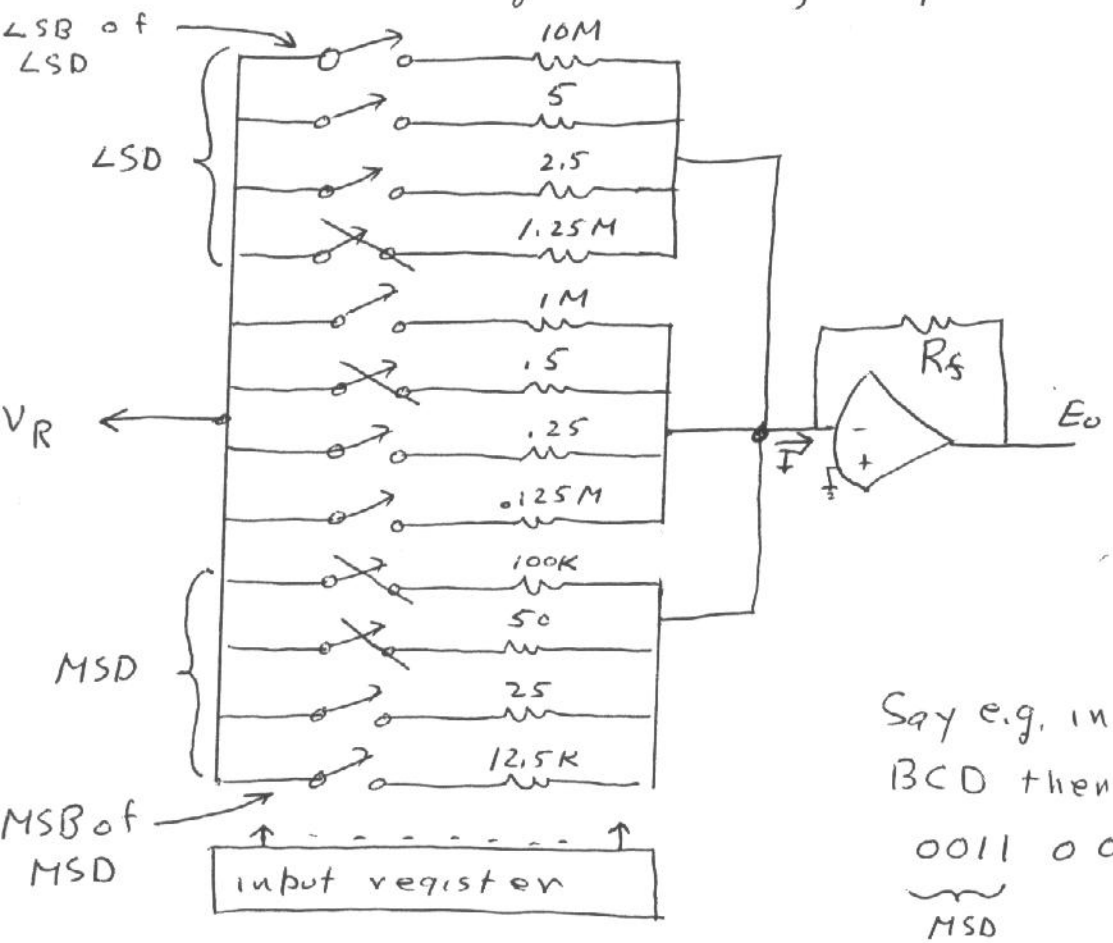


Figure 15.2-4 Output of 4-bit D/A converter with $V_R = 16$ V when connected to a 4-bit counter.

Drawback 1.+2. easily taken care of by using an OA.

" 4. just supply a latching register

Drawback 3 (resistor value range) fairly important, and can become even more so if use different weighting scheme. e.g. BCD weighting as in



Say e.g. input is decimal 328

BCD then is:

0011 0010 1000

MSD LSD

Then switches in RED closed and current injected is

$$I = V_R\left[\frac{1}{50} + \frac{1}{100} + \frac{1}{500} + \frac{1}{1250}\right]10^{-3} = V_R\left(3.28 \cdot 10^{-5}\right)$$

and if choose $V_R = 10v$ and $R_f = 10K\ (=10^4)$ get:

$$E_o = -R_f \cdot I = -10^4\,(10)\left(3.28 \cdot 10^{-5}\right) = 3.28\ v$$

Hence so far $I_T = \frac{V_R \cdot X_3}{2R} + \frac{V_R \cdot X_2}{4R}$

this contribution is $\frac{1}{2}$ that of next higher order bit

Home exercise:

Show that contributions from cases where only X_1, X_0 are on will be respectively,

$$I_1 = \frac{V_R \cdot X_1}{8R} \quad \text{and} \quad I_0 = \frac{V_R \cdot X_0}{16R}$$

Summing all contributions the total current into the OA will be

$$I_{tot} = \frac{V_R}{R}\left[\frac{X_0}{16} + \frac{X_1}{8} + \frac{X_2}{4} + \frac{X_3}{2}\right]$$

For output of OA choose e.g. $R_S = 2R$ to get:

$$-E_o = R_S \cdot I_{Tot} = 2R \cdot I_{Tot} = V_R\left[\frac{X_0}{8} + \frac{X_1}{4} + \frac{X_2}{2} + \frac{X_3}{1}\right]$$

take e.g. $V_R = 8\,v$ and input $\overset{X_3}{0}\,1\,1\,1\overset{X_0}{}$, then get

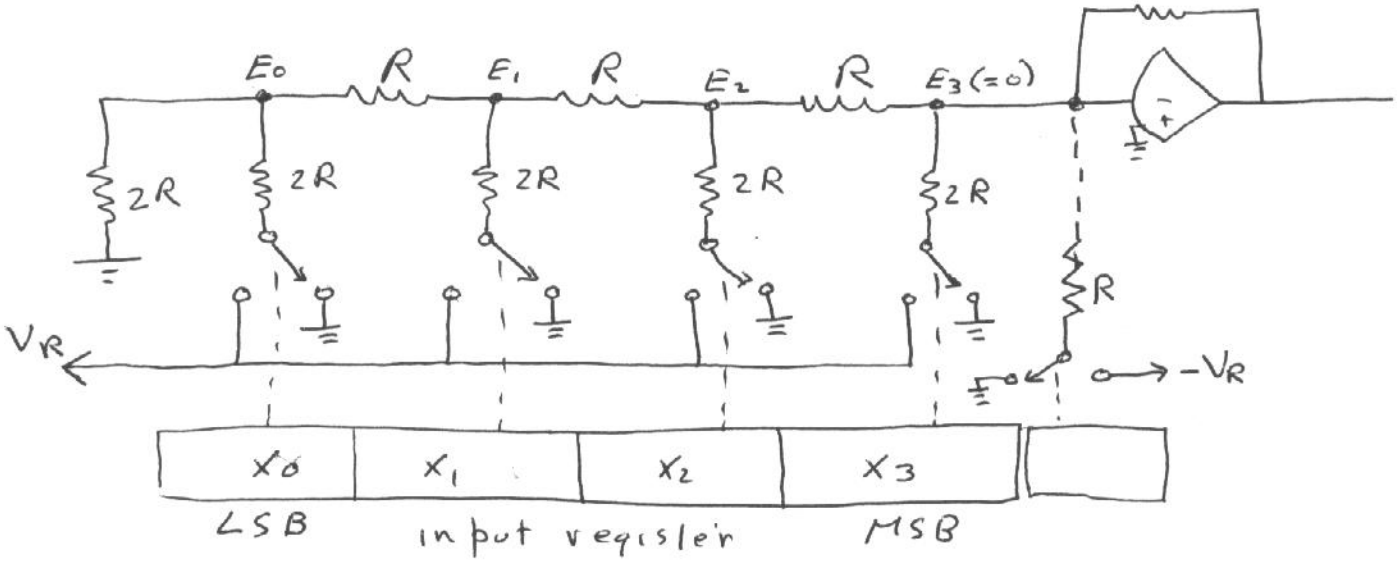
$$-E_o = 8\left[\frac{1}{8} + \frac{1}{4} + \frac{1}{2} + \frac{0}{1}\right] = 8\left(\frac{7}{8}\right) = 7\,v$$

Now consider the dotted input which can switch $-V_R$ into the S.P. through R, controlled by additional bit X_4.

R is half the size of 2R so it would contribute twice as much current. Hence get

$$-E_o = 8\left[\frac{X_0}{8} + \frac{X_1}{4} + \frac{X_2}{2} + \frac{X_3}{1} - 2 \cdot \frac{X_4}{1}\right]$$

The R-2R Ladder: commonly used, with variations, to avoid having large range of resistor values.

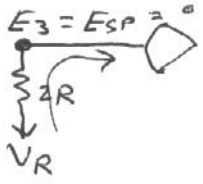


Note switches go to fixed potential low impedance points, either ground or power supply.

Hence the impedance seen looking to left at any node is always 2R

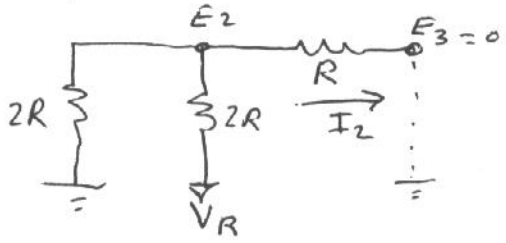
Current contributions gotten by superposition:

1. If only MSB is on (i.e. $X_3 = 1$, $X_{0,1,2} = 0$) then have

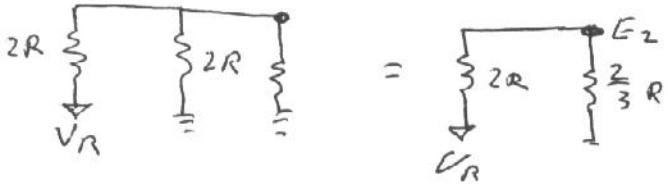


$$I_3 = \frac{V_R}{2R} \cdot X_3$$

2. If only next MSB is on (i.e. $X_2 = 1$, $X_{0,1,3} = 0$) then have



$$I_2 = \frac{E_2}{R} =$$



$$= E_2 = \frac{2/3}{2 + 2/3} V_R = \frac{2}{6+2} V_R = \frac{V_R}{4}$$

hence $I_2 = \frac{V_R \cdot X_2}{4R}$

Now assume have input word 0 0 1 1 1 (one bit longer since x_4 has been added]

Take 2's complement $\underset{x_4}{0}\ 0\ 1\ 1\ 1\ \underset{x_0}{} \rightarrow 1\ 1\ 0\ 0\ 0$

$+1$

$1\ 1\ 0\ 0\ 1$

new x_4 --- x_0

and use this as the DAC input: get

$$-E_o = 8\left[\frac{1}{8} + \frac{0}{4} + \frac{0}{2} + \frac{1}{1} - 2\cdot\frac{1}{1}\right] = 8\left[\frac{1}{8} - 1\right] =$$

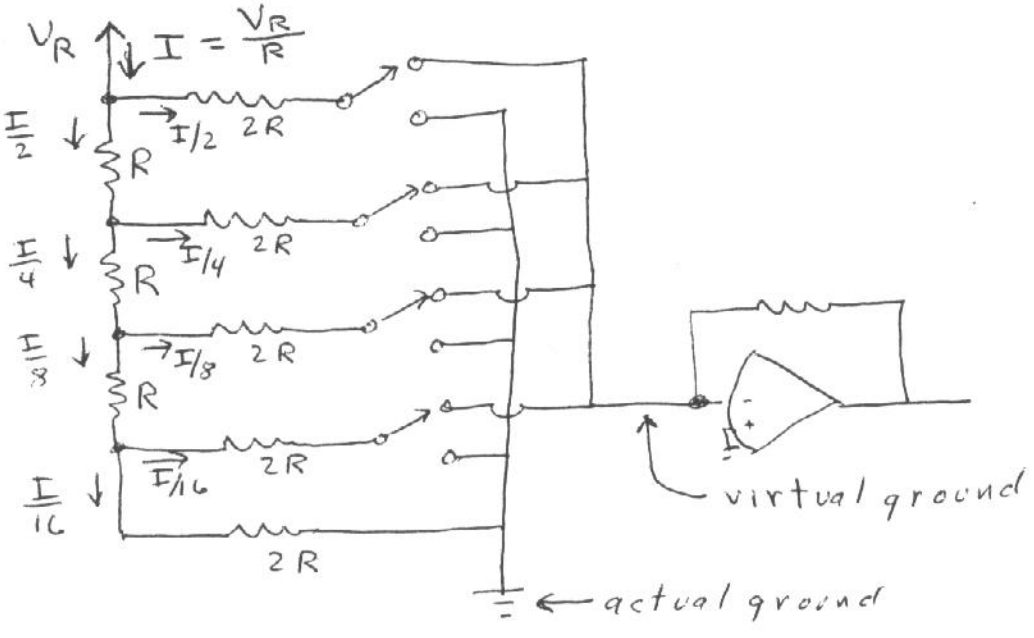
$$= 8\left[-\frac{7}{8}\right] = -7 \text{ volts}$$

Hence DAC can be <u>bipolar</u> using 2's complement representation for the input.

Of course could also use a sign bit and a switched inverter

Inverted ladder variation:

A more common variation of previous version keeps the current thru the "2R" resistors more or less constant and switches it either to actual ground or virtual ground.

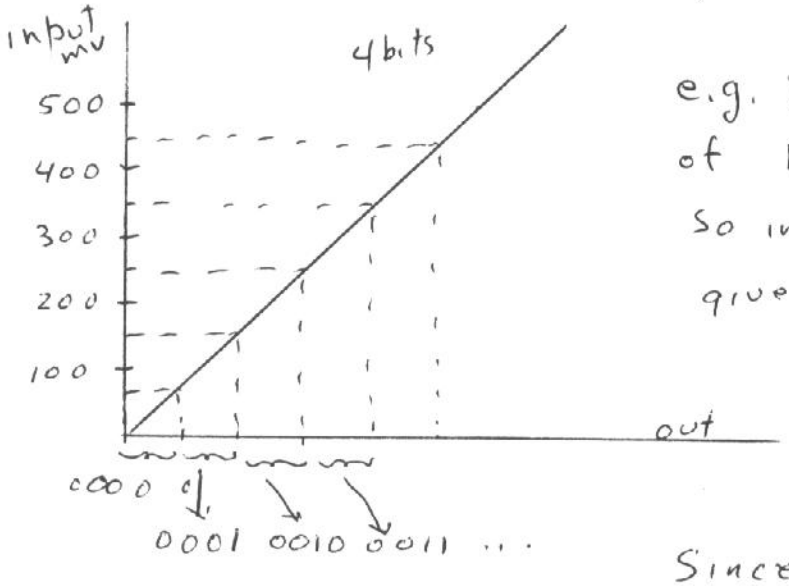


Note that current thru each input "2R" does not change — switched to either true ground or virtual ground. Implies no voltage change across them so no charging and discharging of parasitic capacitances which in turn means faster operation is possible.

Also note that commercial DAC's typically use transistor current sources to supply the various current contributions that are switched in or out. MDAC's

A/D Conversion

A/D circuits accept an analog input and output an N bit word characterizing the analog value. The converters can have errors to be recognized, e.g. Quantization error: analog values within a certain range will all give the same digital output word.



e.g. here have A/D with resolution of 1 count/100 mv in.

So inputs between say 250 mv → 350 mv give same output 0011.

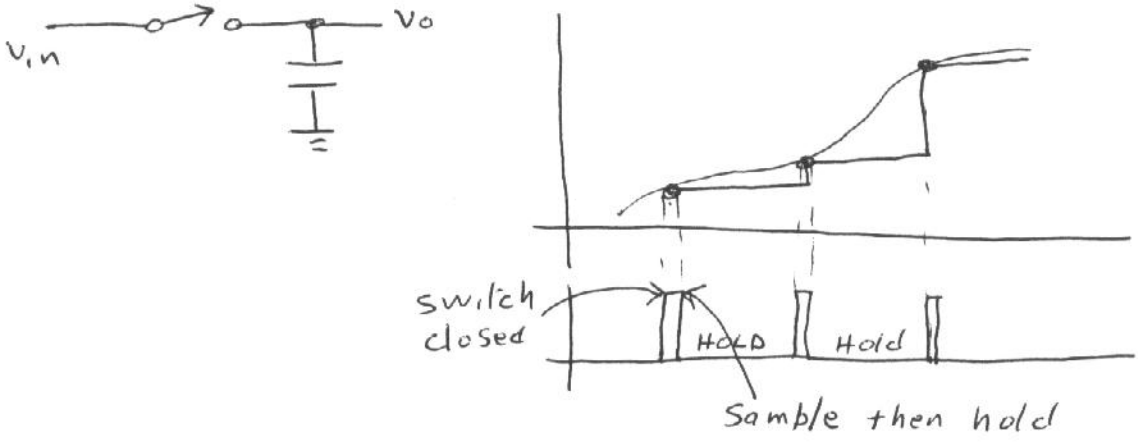
Now if this way inputted to a DAC, it's analog output would be 300 mv.

Since original was in range 250-350 the quantization error would likely be specified as ± 50 mv $= \pm \frac{1}{2}$ LSB

resolution vs accuracy: resolution only indicates what the best theoretical accuracy can be, the more bits the better the resolution. However the overall accuracy depends on components used, stability of any voltage references used, etc,

Time skew error: if the analog voltage input changes during the time conversion is taking place can get errors — hence either have fast converters or use a sample/hold circuit (S/H).

S/H often is in front of an A/D converter, especially if the converter is multiplexed across a number of input channels. Conceptually have e.g.



Two other items often added in front of an A/D are:

Filter - to get rid of noise and/or bandlimit the input

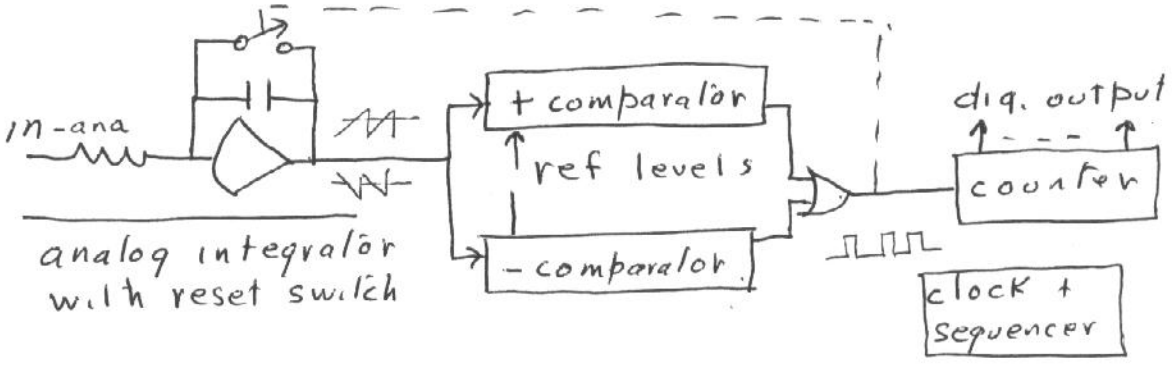
Pre-amp - to bring input levels to more suitable ranges

Absolute magnitude circuit (plus comparator for sign) to supply only uni-polar signals to converter.

Types of ADC's: obviously many ways to classify. For our purposes can consider two broad categories

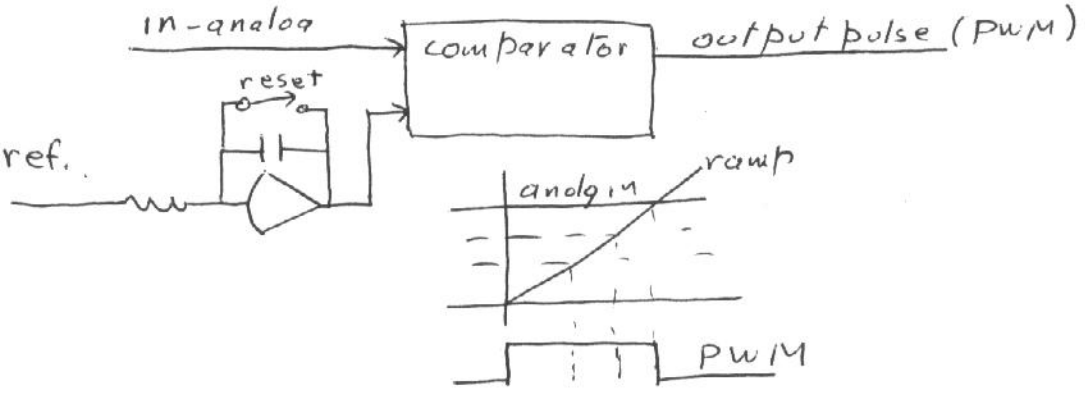
1. Types where no local analog value is generated. Not too common and can be regarded as some form of modulation scheme. e.g.

a. V/F converter - input analog value generates a pulse train



Integrate to ref. level of comparator which generates pulse to increment counter and reset integrator. Count for fixed time and counter output is digital equivalent.

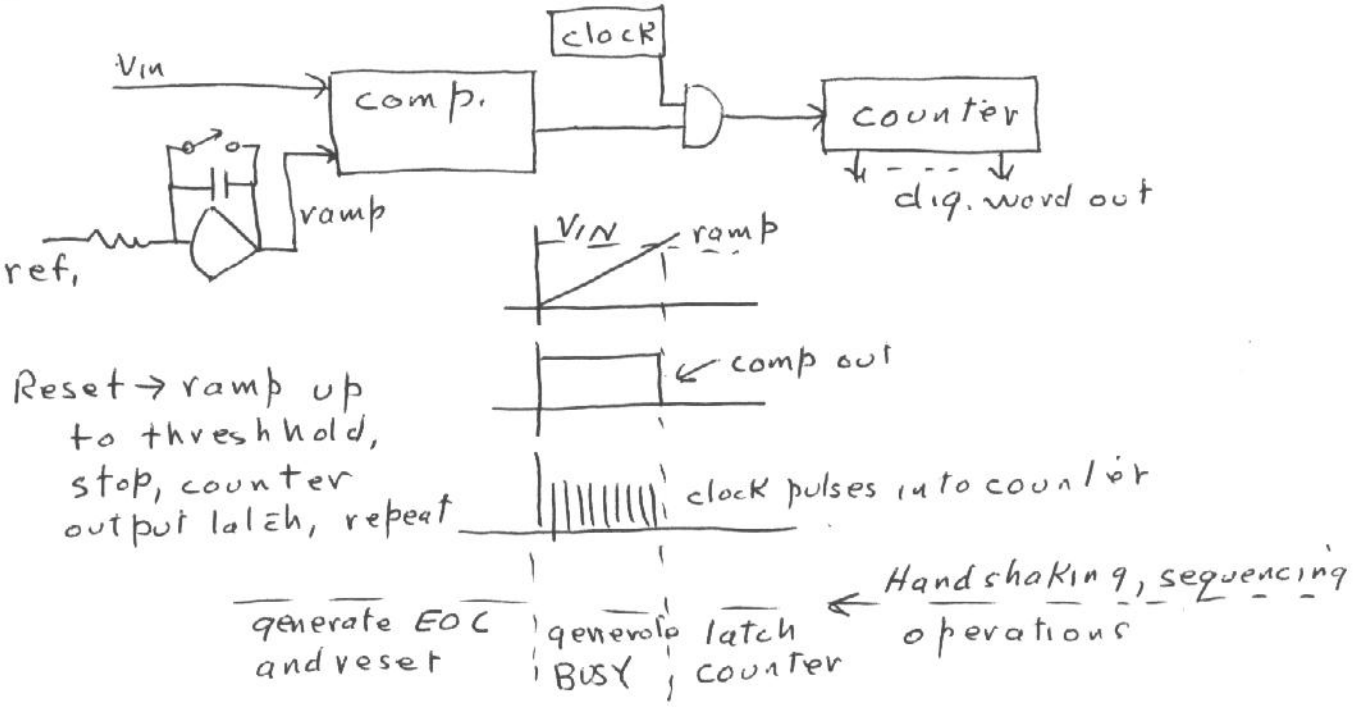
b. PWM (pulse width modulation)



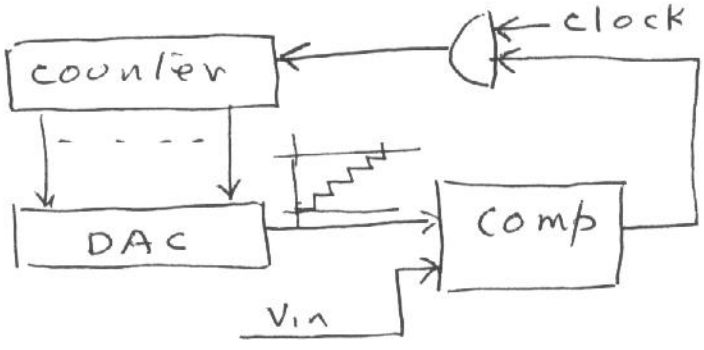
c. Parallel converter - later

2. Types where a local analog valve is generated and compared to input. (often called "balancing" schemes)

a. Open loop ramp - ramp generated analog way (similar to PWM)



b. Open loop ramp - ramp digitaly generated

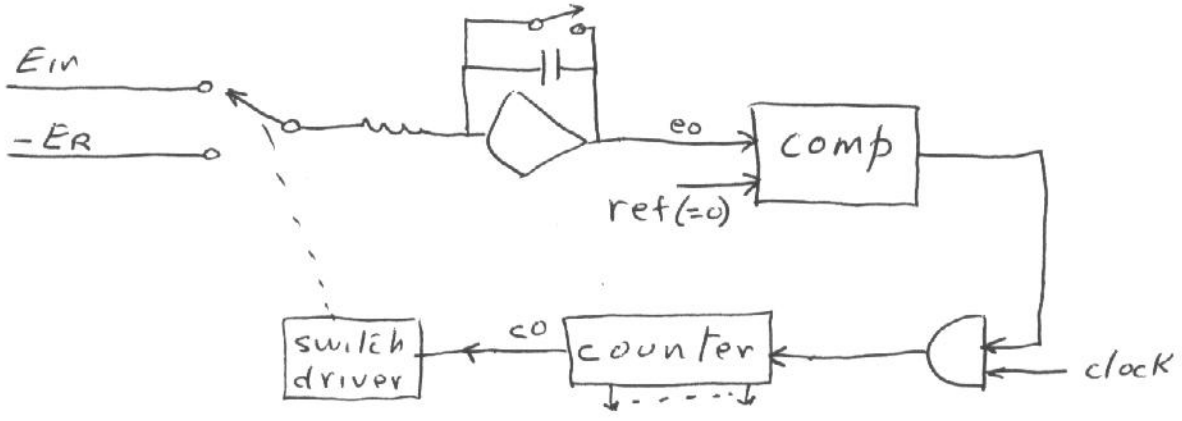


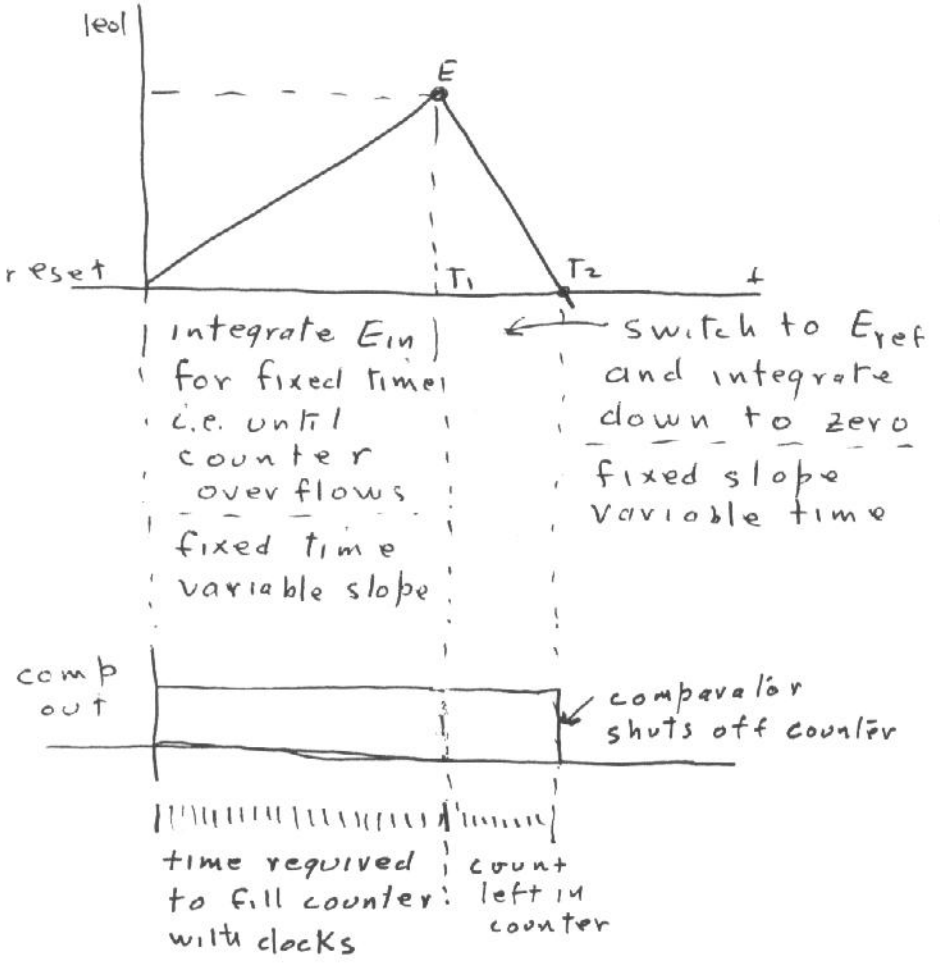
Basically same as 2a. except uses a DAC instead of an analog integrator.

c. Closed loop ramp:

Basically same as above except continuous cycling around analog value with comparator telling counter to count UP or Down. (Has tendency to hunt on noisy input. Faster than open loop.)

d. Dual slope: quite common in things like multimeters.





Note: Main drawback is that it is slow

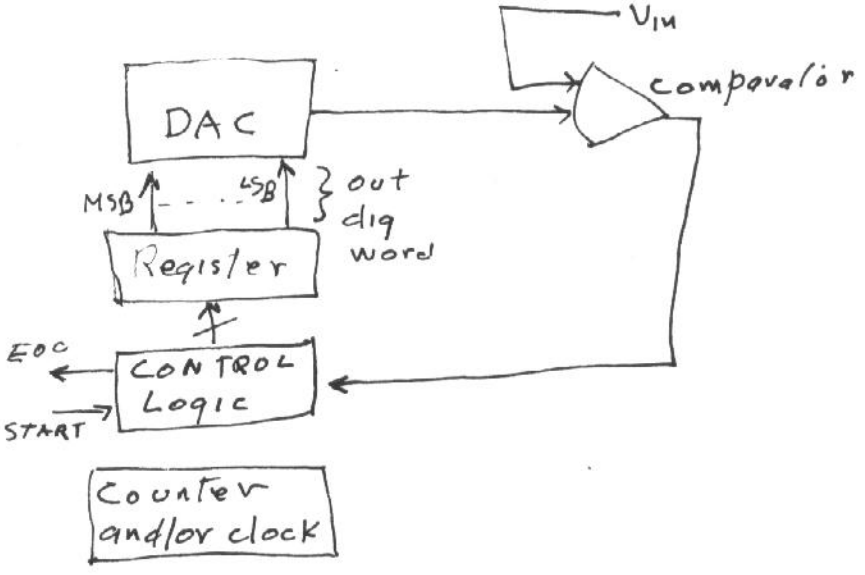
Good features are 1) low cost 2) averages out noise during conversion period 3) independent of R, C, clock period, amp. offset as long as these don't change during conversion cycle.

Can add an auto-zeroing ckt if desired.

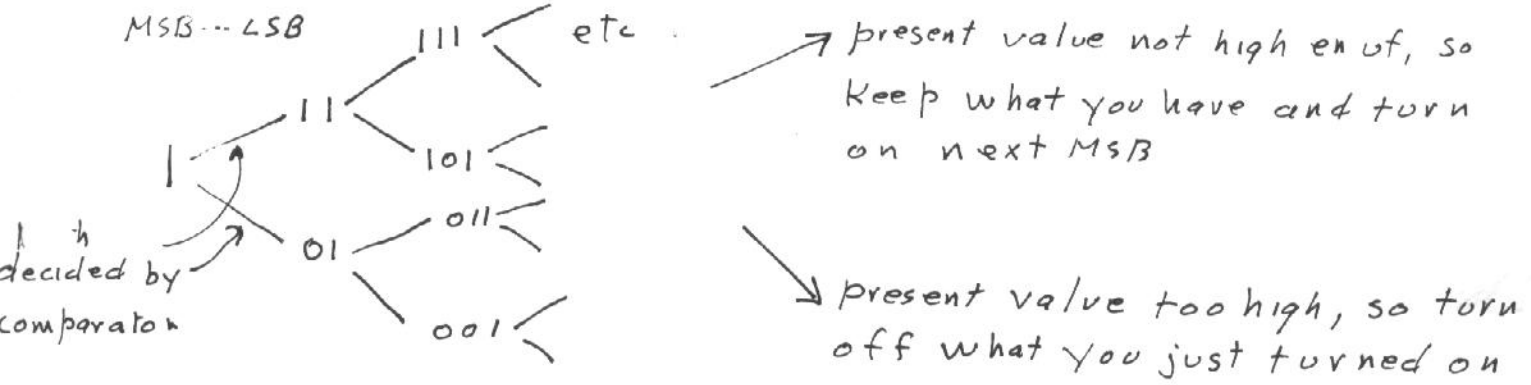
e. SAR (successive approximation register) Converter

Very common, scalable, reasonably fast, reasonable cost

Basic components are a comparator, a DAC, a register, clock and control logic. Block diagram is:



Reset, then turn on MSB in register which generates an analog value ($\frac{1}{2}$ full scale) from the DAC. This is compared to the input. If generated value is not large enough - then keep MSB on and turn on next MSB. If generated value is too ~~small~~ large - then turn off MSB and turn on next MSB. Continue thru all states of the register, generate an EOC and wait for next START command.



5. Flash (AKA parallel) converter: no local analog copy generated. V_{in} simultaneously compared to $2^N - 1$ reference values (i.e. $2^N - 1$ comparators used) which are:

(N = # of bits) $\quad \frac{V_R}{2^N}$ = value of the LSB

ref values set at $\frac{1}{2}\frac{V_R}{2^N}$, $\frac{3}{2}\frac{V_R}{2^N}$, $\frac{5}{2}\frac{V_R}{2^N}$ ... $\left(2^N - \frac{3}{2}\right)\frac{V_R}{2^N}$

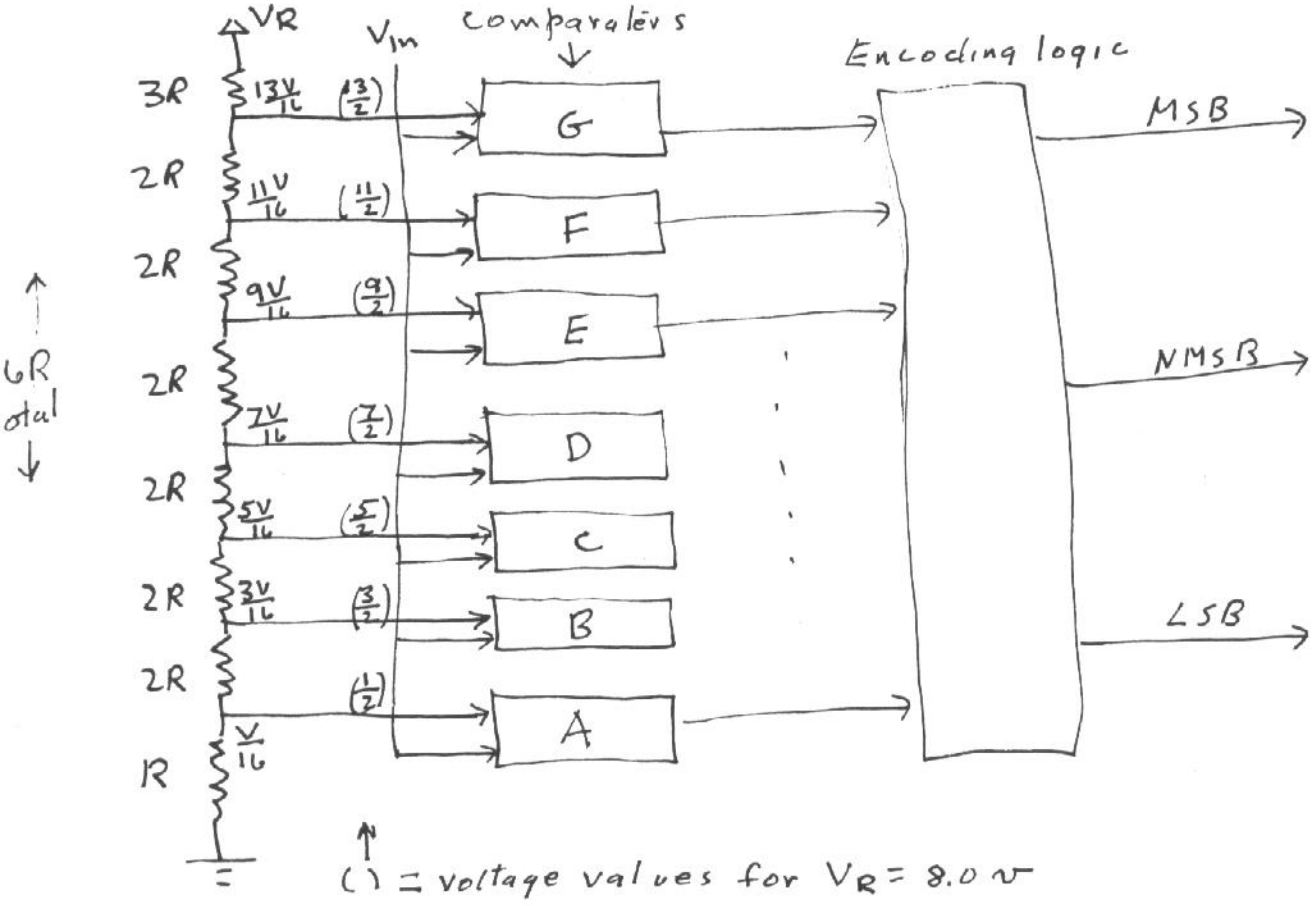
e.g. for $n=3$ and $V_R = 8v$ have $\frac{V_R}{2^3} = \frac{8}{8} = 1v$ = LSB

and thresholds for the comparators are:

$\frac{1}{2}\frac{V_R}{8}$, $\frac{3}{2}\frac{V_R}{8}$ ... works out to

$\frac{V_R}{16}$, $\frac{3V_R}{16}$, $\frac{5V_R}{16}$, $\frac{7V_R}{16}$, $\frac{9V_R}{16}$, $\frac{11V_R}{16}$, $\frac{13V_R}{16}$

and could be built as



Encoding logic:

Input signal level	A	B	C	D	E	F	G	output word MSB	NMSB	LSB
$> 6\frac{1}{2}$	1	1	1	1	1	1	1	1	1	1
$5\frac{1}{2}$ to $6\frac{1}{2}$	1	1	1	1	1	1	0	1	1	0
$4\frac{1}{2}$ to $5\frac{1}{2}$	1	1	1	1	1	0	0	1	0	1
$3\frac{1}{2}$ to $4\frac{1}{2}$	1	1	1	1	0	0	0	1	0	0
$2\frac{1}{2}$ to $3\frac{1}{2}$	1	1	1	0	0	0	0	0	1	1
$1\frac{1}{2}$ to $2\frac{1}{2}$	1	1	0	0	0	0	0	0	1	0
$\frac{1}{2}$ to $1\frac{1}{2}$	1	0	0	0	0	0	0	0	0	1
0 to 1/2	0	0	0	0	0	0	0	0	0	0

exercise, get MSB = and draw ckt

NMSB =

LSB =

Flash converters = fastest type

= many comparaters ⇒ high cost